Remarks and Arguments

The drawings were objected to because Figure 2 includes reference numeral 270 that was not described in the written specification. The specification has been amended at page 14 to include a reference to numeral 270. This objected is therefore traversed.

Claims 1-26 were presented for examination. Claims 2-5, 8, 11-13, 15,-17, 20 and 22-26 have been amended. Claims 1, 6-7, 9-10 and 18-19 have been canceled. Claims 27-30 have been added.

Claim 22 has been objected to because two claims have the number "22." The second claim numbered "22" has been changed to claim "26."

Claims 17 and 20 have been rejected under 35 U.S.C. §112, second paragraph, for lack of antecedent basis for the phrases "The memory controller" and "said controller processing core" (claim 17) and "said rechecking information" (claim 20.) In response, claim 17 has been amended to be dependent on claim 13. The phrase "The memory controller" finds antecedent basis on line 1 of claim 29, on which claim 13 depends. The phrase "said controller processing core" finds antecedent basis in line 3 of claim 13.

Claim 20 has been amended to delete the phrase "said rechecking information" and the rejection is now moot.

Claims 1, 2, 4, 6, 7, 9-11, 16-21, 24 and 25 were rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No 5,371,745 (Kiyonaga.) The examiner comments that the cited reference discloses all of the recited elements.

The present invention is a computer memory error management system and method that attempts to correct memory errors in a manner that permits smooth and continuous operations. In one embodiment, when an error is detected in information read from a memory location, a determination is first made whether the error is correctable.

If the error is correctable, it is corrected and the memory location is "refreshed" by rewriting the corrected information back into the same location from which the erroneous information was read. The location is reread and the information is again checked for errors. If there are no errors in the reread information, then the error was assumed to be a soft error and a soft error routine is initiated (for example, logging the error.)

Alternatively, if the reread information has an error, the error is assumed to be a hard error caused, for example, by a hardware failure. In this case a hard error routine is initiated which may take the form of writing the corrected information to another memory location or starting a failover process in which another memory controller handles the read and write process.

If the error was initially determined to be non-correctable, then a non-correctable error process is initiated. This may, for example, entail reading the information from an alternate source and writing the new information into another memory location or starting a memory controller failover process as previously described.

The Kiyonaga reference discloses an error correction apparatus for use with tape drives. In this system, information from a tape location is read and error detection is performed on the information. If an uncorrectable error is detected, the tape is rewound and the information is reread from the tape location. The error detection and correction procedure is performed again in the hopes that the error was caused by dirt, etc. which would be dislodged during the reread operation. This type of operation is known as a "read retry" and is described at Kiyonaga column 1, lines 46-60. The invention disclosed in Kiyonaga relates to a more sophisticated determination whether a read retry should be initiated. This more sophisticated determination involves partial retry determining circuits and retry determining circuits. However, after a determination is made whether a retry should be performed, the retry performed in Kiyonaga is still a read retry.

In contrast, the "retry" of the present invention involves correcting an error that is correctable and then rewriting the corrected information into the location from which it was read. The rewritten information is then reread to determine whether errors are still present. This operation is recited in new claim 27, which replaces original claims 1, 6 and 7. For example, new claim 27 recites, in lines 4-9, "if a correctable error exists in the information, correcting the error in the information, rewriting the corrected information back into the memory at the location and rereading information from the error checking and correction memory at the location to determine whether the correctable error has been corrected. No such operation is disclosed in the Kiyonaga reference. Consequently, new claim 27 patentably distinguishes over the cited

Kiyonaga reference.

Claims 2 and 4 have been amended to make them dependent on new claim 27 and incorporate the limitations thereof. Therefore, they distinguish over the cited reference in the same manner as new claim 27.

Similarly, new claim 29 has been added, which replaces original claims 9 and 10. Claim 29 recites, in lines 5-13, "an error detector that responds to the information by determining whether a correctable error exists, a soft error corrector that cooperates with the error detector by correcting the correctable error in the information, a memory refresher that writes the corrected information back into the memory at the location and a checker that cooperates with the memory refresher to cause the reader to read information from the memory controller buffer at the location to determine whether the correctable error has been corrected." . No such apparatus is disclosed in the Kiyonaga reference. Consequently, new claim 29 patentably distinguishes over the cited Kiyonaga reference.

Claims 11, 16 and 17 have been amended to make them dependent on new claim 29 and incorporate the limitations thereof. Therefore, they distinguish over the cited reference in the same manner as new claim 29.

New claim 30 has been added, which replaces original claims 18 and 19. Claim 30 recites, in lines 4-8, "if a correctable error exists in the information, correcting the error in the information, rewriting the corrected information back into the memory at the location and rereading information from the error checking and correction memory at the location to determine whether the correctable error has been corrected..." No such operation is disclosed in the Kiyonaga reference. Consequently, new claim 27 patentably distinguishes over the cited Kiyonaga reference.

Claims 20, 21, 24 and 25 have been amended to make them dependent on new claim 30 and incorporate the limitations thereof. Therefore, they distinguish over the cited reference in the same manner as new claim 30.

Claims 3, 8, 13-15 and 22-23 have been rejected under 35 U.S.C. §103(a) as obvious over Kiyonaga in view of U.S. Patent No. 6,154,850 (Idleman.) The examiner comments that Kiyonaga discloses all of the recited limitations except that Kiyonaga does not disclose that the memory is a memory controller buffer for a disk array.

However, the examiner asserts that the Idleman reference discloses memory controllers for both disk arrays and tape drives. The examiner concludes that it would have been obvious to combine the teachings of Kiyonaga and Idleman in order to interface a computer with a storage system, such as a disk or tape system by using memory controllers.

The Idleman reference discloses a tape backup system in which data is spread over a set of tape drives in order to reduce the time needed to compute error correcting information. In particular, a block of data to be stored on the tape is split into several smaller sub-blocks, each of which is stored on a separate tape drive. Error correcting information is then computed for each of the sub-blocks. Since each sub-block is smaller than the original data block, the time required to compute the error correcting information is less than the time required to compute error correcting information for the original data block. Because the error correcting information for the sub-blocks is computed in parallel, the overall time for computing the error correcting information is reduced. In addition, the use of multiple tape drives allows information to be recovered from a failed tape drive in much the same manner as information can be recovered from a failed disk drive in a RAID system. Idleman also shows the use of two controllers that are arranged in a fail over configuration so that, if one controller fails, the other controller can take over control of the system.

Claims 3 and 8 depend from claim 27 and incorporate the limitations from claim 27. As discussed above, claim 27 distinguishes over Kiyonaga because Kiyonaga does not disclose correcting information that was read in error and rewriting the corrected information in the same location. However, the Idleman reference does not disclose details of correcting information read from the disk or tape drives using the error correcting information. Specifically, it does not disclose correcting information that was read in error and rewriting the corrected information in the same location. Instead, Idleman discloses reconstructing the data on an entire failed tape drive on another drive and replacing the failed tape drive with the other drive.

Consequently, the combination of Idleman with Kiyonaga cannot teach or suggest the combination claimed in claims 3 and 8 because neither reference discloses the error correcting process claimed in these claims.

In a similar manner, claims 13-15 depend on claim 29 and incorporate the limitations thereof. Therefore they distinguish over the cited references in the same manner as claim 29. Claims 22-23 depend on claim 30 and incorporate the limitations thereof. Therefore they distinguish over the cited references in the same manner as claim 30.

Claim 5 has been rejected under 35 U.S.C. §103(a) as obvious over Kiyonaga in view of U.S. Patent No. 6.308,680 (Olarig.) The examiner comments that Kiyonaga discloses all of the recited limitations except that Kiyonaga does not disclose the use of Hamming codes and error syndromes to correct errors. However, the examiner asserts that Hamming codes are disclosed in the Olarig reference and that it would have been obvious to use Hamming codes as taught by Olarig instead of the parity scheme taught by Kiyonaga.

The Olarig reference discloses a dual memory sub-system with automatic failover from one memory to the other when a fault is detected. The failover is conducted while the system is in operation under control of a state machine. While the Olarig reference does disclose the use of various error correcting codes, such as Hamming and Reed-Solomon codes for error correction, it does not disclose details of the error correction process and does not disclose correcting information that was read in error and rewriting the corrected information in the same location.

Consequently, the combination of Kiyonaga with Olarig cannot teach or suggest the combination claimed in claim 5 because neither reference discloses the error correcting process claimed in this claim.

Claims 12 and 26 have been rejected under 35 U.S.C. §103(a) as obvious over Kiyonaga in view of U.S. Patent No. 6,477,662 (Beffa.) The examiner comments that Kiyonaga discloses the claimed limitations except for the process of fencing off a location in the memory after a failure has been detected. The examiner asserts that Beffa teaches isolating defective locations in a failed memory and that it would be obvious to use this technique to force a rewrite of a failed location.

While the Beffa reference does disclose fencing off failed locations in a memory, it does not discuss correcting data read from a location and them rewriting the corrected information into that location. Instead, information read from a memory cell is

determined to contain errors by comparing the information read from the cell with the test information used to write that cell (See Beffa, column 5, lines 41-49. Once a cell is determined to be defective, it is permanently removed from operation by substituting a row or column for the row or column containing the failed cell. Alternatively, bocks of cells containing a failed cell can be removed from operation by isolating them by the "partialing" process described at column 7, lines 18-28. However, Beffa does not disclose details of the error correction process and does not disclose correcting information that was read in error and rewriting the corrected information in the same location.

Consequently, the combination of Kiyonaga with Beffa cannot teach or suggest the combination claimed in claims 12 and 26 (which are dependent on claims 29 and 30, respectively) because neither reference discloses the error correcting process claimed in these claims. Consequently claims 12 and 26 distinguish over the cited references in the same manner as claims 29 and 30.

New claim 28 was added to cover the non-correctable error process described at page 23, line 11 to page 24, line 5.

Based on the above discussion, claims 2-5, 8, 11-17 and 20-30 are allowable and advancement of this application to issue is respectfully requested. The Commissioner is hereby authorized to charge any fees or credits under 37 C.F.R. §1.16 and 1.17 to our deposit account No. 02-3038.

Respectfully submitted

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